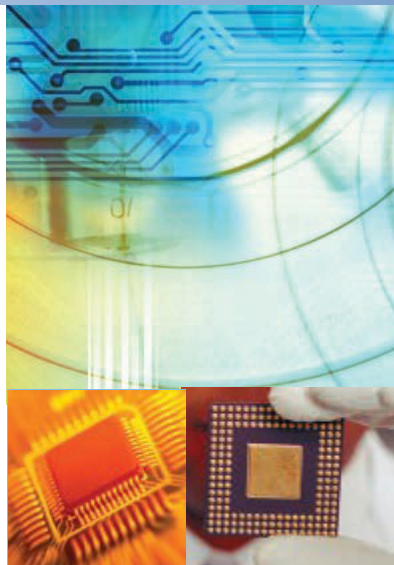


Thermo Scientific MK.1 ESD and Static Latch-up Test System

The Thermo Scientific MK.1 is a relay-based, exceptionally fast ESD and Static Latch-Up Test System used in the evaluation of advanced IC devices. It fully addresses today's JEDEC/ESDA standards, and can be configured with 64, 128, 192 or 256-pin test capabilities.

- Waveform network: 8-site HBM pulse source
- Human Body Model (HBM) and Machine Model (MM) testing to industry standards
- Static Latch-Up testing per current JEDEC's EIA/JESD 78 method
- Highly repeatable, reproducible test data
- Enhanced data set features
- High voltage power supply chassis
- Power supply sequencing
- Event trigger output
- Intuitive set-up and operation using the Thermo Scientific™ Scimitar™ software platform
- Direct use of existing 256 pin-style ZapMaster fixtures



Rapid, High-throughput Testing of Complex IC Devices, from Design through Post-production Qualification

The Thermo Scientific™ MK.1 ESD and Static Latch-up Test System provides users with advanced capabilities to test mid-range pin count devices to today's Human Body Model (HBM) and Machine Model (MM) ESD standards. The system's pulse delivery design ensures recently identified waveform hazards in the standards, such as the trailing pulse and the pre-discharge voltage rise are addressed.

Trailing pulses were shown to cause non-ESD related failures by exposing the DUT to an electrical overstress after the main HBM event. Pre-discharge voltage can cause voltage-triggered protection structures to fail, as the pin under test may not be at zero volts when the HBM event occurs. A user-selectable 10K Shunt can be connected



during the pulse to eliminate any voltage prior to the actual HBM event. A combination test system, today's MK.1 test system also performs Static Latch-Up testing per JEDEC's EIA/JESD 78 method.

Easy-to-Use Testing Operations

The MK.1 Scimitar Windows®-based software is both intuitive and comprehensive. Tests are set-up quickly, and user training requirements are minimal. A powerful embedded VME controller handles an enormous amount of test program and result data, while controlling the system hardware.

Consistent, Precise ESD Waveforms

By locating multiple discharge networks close to the test fixture board, unwanted stray inductance and capacitance is kept to a minimum at every pin. This ensures excellent in-test waveform quality and easily reproducible test data.

Define, Achieve and Sustain Your Test Objectives

The MK.1's flexible, modular design and options enable you to upgrade on-site when corporate or industry standards change. Options include additional pins, bias supplies, and static latch-up. The MK.1 design and matrix layout allows the direct use (no adapter required) of 256-pin-style ZapMaster fixtures. Optional carriers are available for centrally mounted sockets. Adapters are also available for 256-pin Verifier DUT boards.

Reach the Next Level of Success

Experience the many benefits of working with recognized experts in the field of component reliability ESD and Static Latch-Up testing. Our goal is to support you with lifelong service — from applications support, calibration services, service contracts, and field service scheduling to full technical field support. We can help you reach that next level of success.

General Specifications

Tests Devices up to 256 pins	Systems available configured as 64, 128, 192, or 256 pins; upgradeable in the field. Additional capability, faster throughput, multi-site testing
Relay-Based Operations	Enables test speeds 5 to 10 times faster than robotic-driven testers
Waveform Network	8-site HBM pulse source with 100pF/1500Ω. Patented design ensures waveform compliance for technology generations to come
High Voltage Power Supply Chassis	Modular chassis with patented HV isolation enables excellent pulse source performance
Power Supply Sequencing	Additional flexibility to meet more demanding test needs of integrated system-on-chip designs
Event Trigger Output	Manage your setup analysis with customized scope trigger capabilities
Human Body Model (HBM)	Per ESDA/JEDEC JS-001-2012, MIL-STD 883E, and AEC Q100-002 specs, 30V to 8kV. Test to multiple industry standards in one integrated system; no changing or alignment of pulse sources
Machine Model (MM)	Per ESDA STM5.2, JEDEC EIA/JESD22-A115, and AEC Q100-003, 30V to 1kV Integrated pulse sources allow fast multi-site test execution
Static Latch-Up Testing	Per JEDEC EIA/JESD 78 and AEC Q100-004. Optional static Latch-Up testing allows control of DUT pins using embedded bias supplies
Up to 4 separate V/I Supplies (1 stimulus and 3 bias)	DUT power, curve tracing, and Latch-up stimulus with 4-wire sensing to the matrix for high accuracy. System design also provides high current capability through the V/I matrix
Multiple Self-Test Diagnostic Routines	Ensures system integrity throughout the entire relay matrix, right up to the test socket
Test Reports	Pre-stress, pre-fail (ESD) and post-fail data, as well as full curve trace and specific data point measurements. Data can be exported for statistical evaluation and presentation
Individual Pin Parametrics	User-defined V/I levels, compliance ranges, and curve trace parameters for each pin individually
Enhanced Data Set Features	Report all data gathered for off-line reduction and analysis; core test data is readily available; all data is stored in an easy- to-manipulate standard XML file structure
Interlocked Safety Cover	Ensures no user access during test. All potentially lethal voltages are automatically terminated when cover is opened. Safety cover window can be easily modified to accept 3rd party thermal heads
Dimensions	57.9 cm (22.8 in) W x 77.5 cm (30.5 in) D x 99.1 cm (39 in) H

Scimitar Software Features

Summary Panel with easy navigation among device components

Wizard-like prompts on multi-step user actions

Control of external devices through the use of Scimitar's user programmable Plug-in capabilities, in addition to the Event Trigger Outputs, which provide TTL control signals for external devices, such as power supplies or for triggering oscilloscopes

Flexible parametric tests that are defined and placed at an arbitrary position within the executable test plan.

Comprehensive results viewer that provides:

- ESD and Static Latch-up data viewing capabilities
- Curves viewer with zooming capabilities and the ability to add user comments
- Data filtering on the following criteria – failed pins, failed results, final stress levels
- A complete set or subset of results using user defined parameters
- Sorting in ascending or descending order by various column criteria

Tree-like logical view of the tests and test plans.

Flexible data storage that provides the ability for the end-user to query the data

Seamless support of existing ZapMaster, MK.2, MK.4, and Paragon test plans

Curve tracing with curve-to-curve and relative spot-to-spot comparison

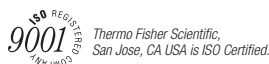
Off-line curve analyzing, including third-party generated waveforms

Canned JESD78A test (static latch-up only) that can be defined automatically

Pause/Resume test capabilities

Intermediate results viewing

Automated waveform capture capability and analysis using the embedded EvalWave software feature



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