

ITWS agenda version 4.13

Day 1 – Sep. 15, 2025

Start	Session	Duration
13:00	Registration and Coffee & Snacks Service	45min
	Distribution of badges etc.	
13:45	Opening Remarks to the ITWS 2025	15min
	Organisational items	
	Speaker: Torsten Liese	
Keynot	e - Al In Our Industry For Testing (Host: Tor	<mark>sten Liese)</mark>
14:00	Keynote: PDF Solutions, USA	30min
	AI For Manufacturing And Test, The New Frontier	
	Speaker: Marc Jacobs	
	Q & A related to this session	
Session	Group A – Automation Processes & Test Solutions From Labs To Fabs (Host: Hara	
14:30	1 st Session: CELADON, USA	30min
	"Innovative On-Wafer PIC Test Solutions for Labs to Fabs"	
	Speaker: Dalton Roehl	
	Q & A related to this session	
15:00	2nd Session: BOSCH Dresden, Germany + ACCRETECH Europe, Munich, Germany	30min
	"The Future of European Wafer Testingan Automation Story"	
	Speaker: Michael Schatterny	
.	Q & A related to this session	
		<mark>ver Nagler)</mark> 30min
15:30	3 rd Session: Delphon, USA + Gel-Pak, USA + CELADON, USA	5011111
	"Extending Parametric Probecard Lifetime To Reduce Overall Cost Of Test For Very	
	Small Pad Probing" Speaker: Garrett Tranquillo (CELADON) & Victoria Tran (Gel-Pak)	
	• Q & A related to this session	
16:00	Coffee Break & Poster Sessions	60min
17:00	4 th Session: CELADON, USA + HTT Group, Germany	30min
17.00	"Recipe for Best-in-Class Production Parametric Testing"	
	Speaker: Karen Armendariz (CELADON) & Janina Freyboth (HTT)	
	• Q & A related to this session	
Session		Host: TBD
17:30	5 th Session: ATV Systems GmbH, Germany	30min
	"1 - Integrated solution for highly stable full wafer reliability testing of microLEDs.	
	2 - VersaJet, an anti-arcing solution from Celadon"	
	Speaker: Ian Cheng	
	Q & A related to this session	
18:00	Cth Consister Destric AC Consister dand	30min
18:00	6 th Session: Dectris AG, Switzerland	
18:00		
18:00	"Session: Dectris AG, Switzerland "Large CMOS Chips Tested on Expanded Frame with Single Die Theta Alignment" Speaker: Pascal Jud	
18:00	"Large CMOS Chips Tested on Expanded Frame with Single Die Theta Alignment"	



Day 2 – Sep. 16, 2025

Start	Session	Duration
Session	Group D – Wafer Testing @ The Limits (Testing @ Hot & Cold Temperature) (Hos	st: TBD)
9:15	7 th Session: University of Basel, Switzerland	30min
	"Cryonic testing Of Quantum Electronic Devices"	
	Speaker: Clemens Spinnler	
	 Q & A related to this session 	
9:45	8 th Session: Session: GlobalFoundries Dresden, + HTT Group, Germany	30min
	"Probing Challenges for High Temperature Testing of MRAM Device"	
	Speaker: Alexander Wittig (GlobalFoundries) & Mike Strech (HTT)	
	Q & A related to this session	
10:15	Coffee Break & Poster Sessions	45min
11:00	9 th Session: ERS Electronic GmbH, Germany	30min
	"Localized Thermal Management for Wafer-Level Testing of High-Power AI and GPU	
	Chips"	
	Speaker: Klaudiusz Holeczek & Klemens Reitinger	
	Q & A related to this session	
Session	Group E – Wafer Testing @ The Limits (High Power/Ultrafast/High Parallelism)	
	(Host: Raine	r Gaggl)
11:30	10 th Session: Infineon Technologies Dresden + JEM Europe, France	30min
	"introduce productive dynamic die-level test (DLT) for SiC FETs, esp. >1kA short-circuit	
	test"	
	Speaker: Andreas Gneupel (Infineon) & Joe Mai (JEM)	
	Q & A related to this session	
12:00	11 th Session: T.I.P.S. Villach, Austria	30min
	"KGD – Ultrafast Dynamic Power Device Probing"	
	Speaker: Sebastian Salbrechter	
	 Q & A related to this session 	
12:30	12 th Session: MPI, Taiwan	30min
	"Structural and Electrical Optimization of Large-Area MLC Probe Card"	
	Speaker: Bobby Chen	
	Q & A related to this session	
13:00	Presentation Awards / Summary of ITWS 2025	30min
	Creaker Territor Line	
12.20	Speaker: Torsten Liese	
13:30	End of Workshop	