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The following subjects should provide inspiration for presentations at ITSW (keynote, on-stage presentations, posters). This is meant to be a non-comprehensive list. If you feel you have a topic to present - related to wafer test - that is not listed below, you are very welcome to propose your abstract as well.

Please note: This is *not* an agenda for the workshop.

- **New Probing Technologies**
  - New/advanced probe card solutions
  - Ultra-fine pitch probing
  - High-pin count / high-parallel probing
  - RF probe cards for wafer-level test (Radar, Lidar, 5G)
  - Photonic probe cards
  - Kryo-probing solutions for quantum computing IC's
- **Advanced Probing Applications**
  - New challenges (tri-temp, power dissipation) for probing & test for automotive IC's
  - WLCSP, module technical challenges for 5G technology (28GHz ~ 44GHz)
  - Wafer handling challenges (thin wafers / thick wafers / non-Silicon wafers etc.)
  - Hot & Cold temperature test
  - MEMS & sensor wafer test
  - BIST & wafer level burn-in
  - Testing of chiplets and substrates
  - Wafer testing with gas
- **Power and Wide-Band-Gap Probing**
  - Highest power (current, voltage)
  - New challenges in testing and handling SiC / GaN wafers
  - Powering AI-chips
- **Probe-Pad/Bump/Pillar Interaction**
  - Challenges for probing over active area
  - Less probe mark damages but good contact – imprint depth – low force probing
  - Probing on Cu/Al/Au/NiP-pads
  - Bump, micro-bump & copper pillars, WLCSP challenges & solutions

- **Prober, Inspection & Metrology Tools**
    - Frame probing with temperatures
    - (Semi-)automatic wafer probing solutions
    - Probe mark inspection (PMI)
    - Probe card analyzing tools
    - Advances in metrology tools
- **Data management and AI**
    - Known Good Die Probing
    - Machine Learning (ML) & Artificial Intelligence (AI) in our industry (for testing)
    - Inline automated process control (tip diameter, CRes, probe marks, etc.)
    - Post vs. inline PMI
    - Probing data management
- **Probing Process and Cost Optimization**
    - Probe cleaning technologies / Probe tip resistance / burn on probe tip / probe cleaning at temp. probing
    - Efficiency during testing by optimized probe card design
    - System level test on wafer level, challenges and solutions
    - Test Synergies - steps forward with cooperations
    - Improving Cost-of-test

Are you interested in giving a presentation on one of these subjects?

Please do not hesitate to contact us via e-mail info@is-test.com or phone!